Centre Français Fiabilité

# NRTW 2025

## National Reliability Technology Workshop

Mercredi 19 et Jeudi 20 mars 2025 | GANIL – Bd Henri Becquerel, 14000 Caen

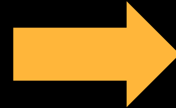
# ENJEUX DE LA FIABILITÉ DES COMPOSANTS EN CONDITIONS EXTRÊMES

Florence MALOU

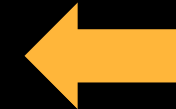
CNES

Organisé par :

# APPLICATIONS EN ENVIRONNEMENTS SÉVÈRES



NOUVEAUX DÉFIS TECHNOLOGIQUES NÉCESSITENT



↗ Intégration

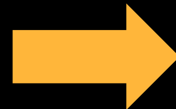
↗ Fonctions

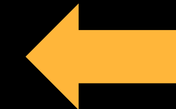
↗ Performance

↗ Robustesse

↘ Consommation

↘ Coût





# FEUILLE DE ROUTE COMPOSANTS

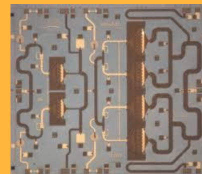
Silicium

FPGA ULTRA 7

Chiplet, UDSM

GaN/SiC Puissance

Convertisseurs A/D



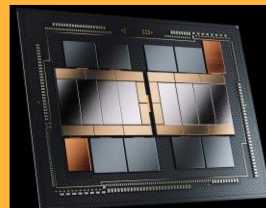
GaN RF mmW

Photonique

Cellules Solaires

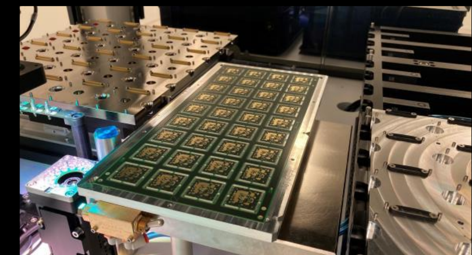
Détecteurs

Passif



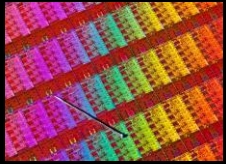
Assemblage & PCB

SiP 2.5D/3D



Moyens d'essais
Fiabilité /Radiation

# LOI DE MOORE

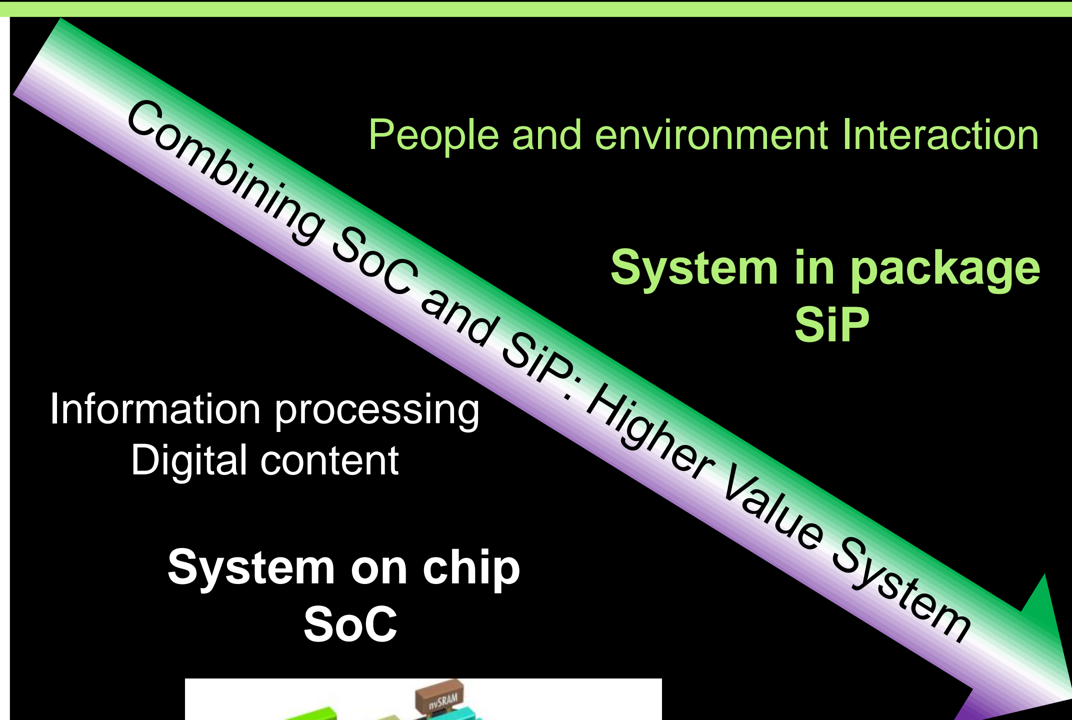


More MOORE miniaturization
baseline CMOS: CPU, memory, logic

130 nm
90 nm
65 nm
45 nm
32 nm
22 nm
7 nm

More than MOORE diversification

Analog/RF Passives HV power Sensors MEMS RFID/NFC



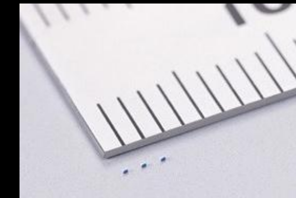
Combining SoC and SiP: Higher Value System

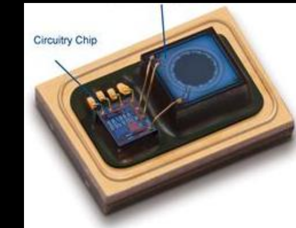
People and environment Interaction

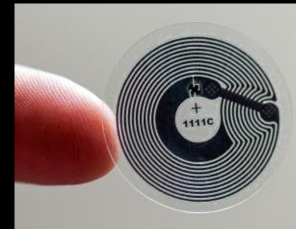
**System in package**
**SiP**

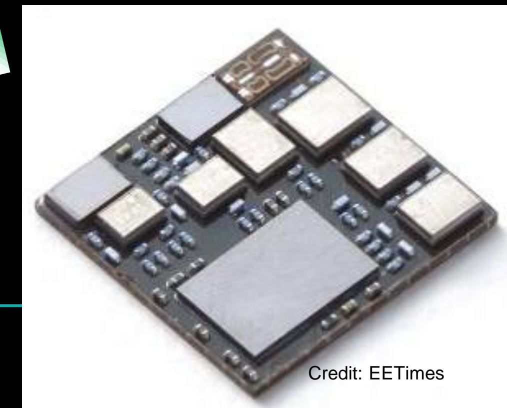
Information processing
Digital content

**System on chip**
**SoC**





Credit: EETimes

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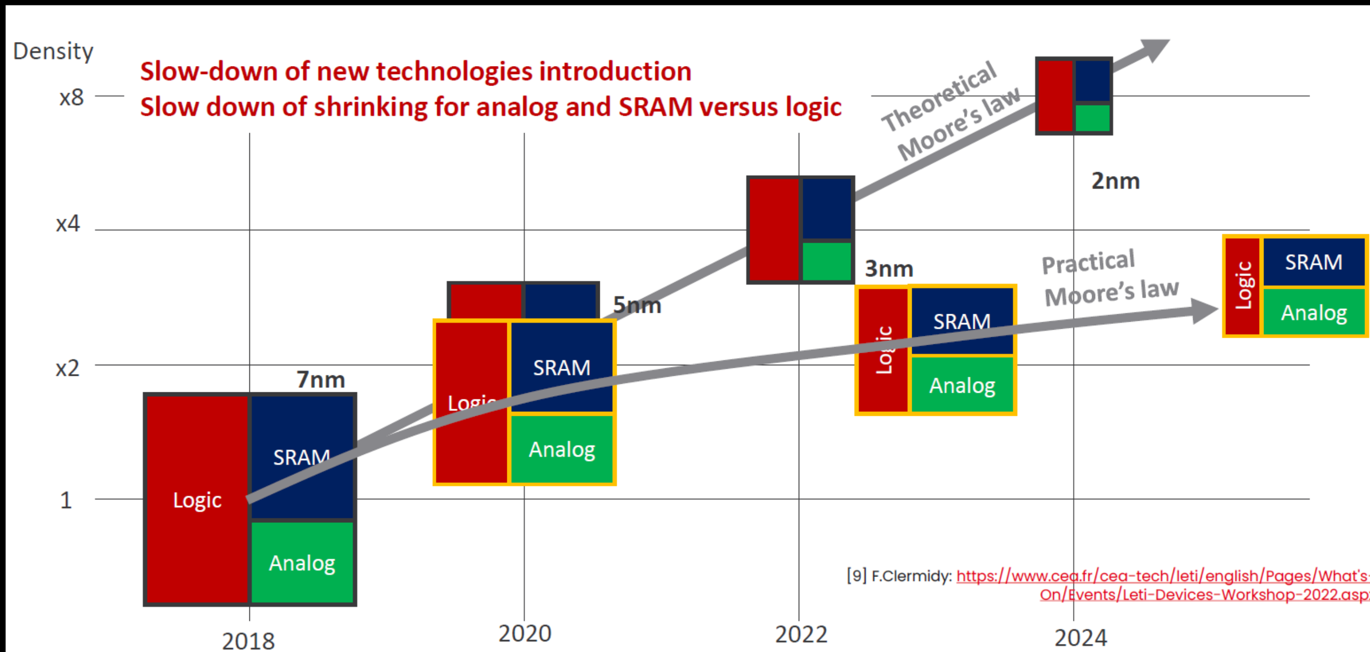
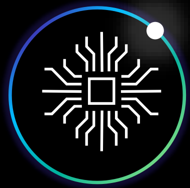
# LA LOI DE MOORE RALENTI



At IEDM 2017, AMD CEO Dr. Lisa Su reported cost per yielded mm² for a 250 mm² die.

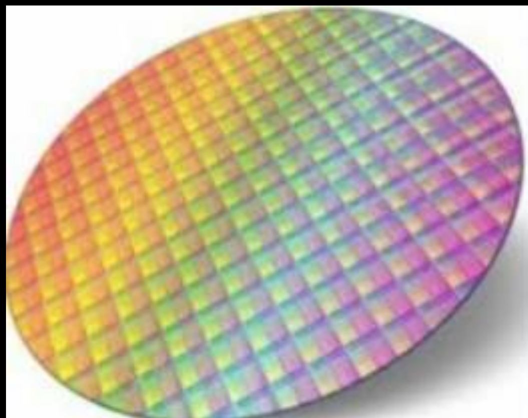
→ Partitionnement Chiplet & Intégration hétérogène

# UN DIFFERENTIATEUR DE COMPETITIVITE : LA TECHNO UDSM (ULTRA DEEP SUB-MICRON)



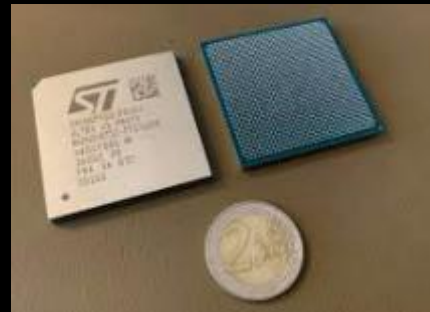
## Déterminant : Finesse de gravure en nm

Impacte directement le nœud technologique & Dimensions Transistor



1 wafer
*(issu d'un run de fonderie)*

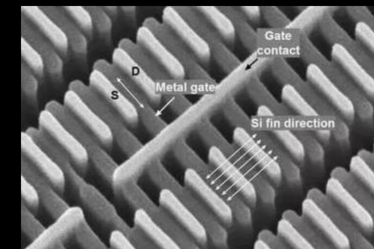
des centaines de puces

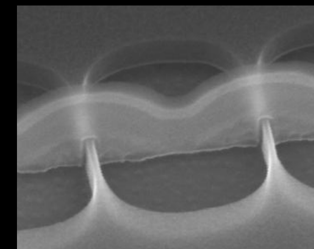



des milliards de transistors

↗ Performance
↘ Consommation

qq nm *



** plus de 1000 fois plus petit qu'un cheveu…*

# MICROÉLECTRONIQUE D'AUJOURD'HUI ET DE DEMAIN

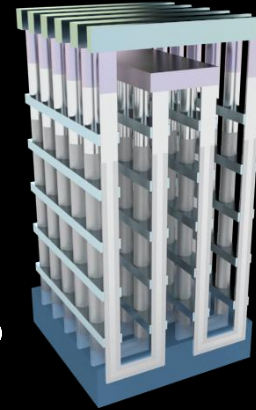
## Solid state Non volatile Storage

- 3D Flash NAND
- Phase-change RAM / PRAM
- Ferroelectric RAM / FeRAM
- Magnetoresistive RAM / MRAM
- Conductive Bridge RAM (CB-RAM)

## Advanced FET transistors

- FinFET
- FD-SOI transistor
- GAA Transistor (Gate All Around)
  - Multi-Bridge-Channel FET (MBCFET – Samsung)
  - Ribbon FET (Intel)
  - Vertical FET (VFET)

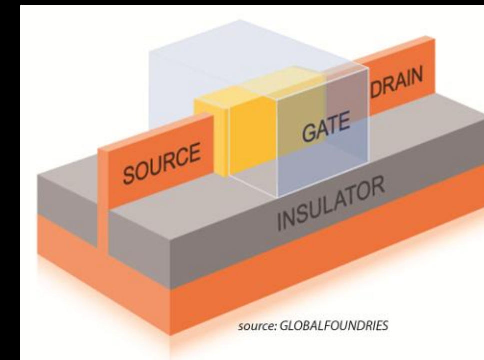
## Chiplet



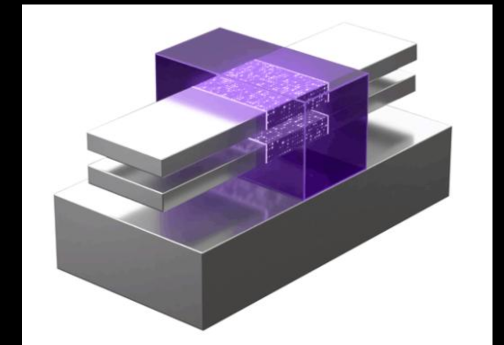
3D Flash NAND

Source : ST Microelectronics

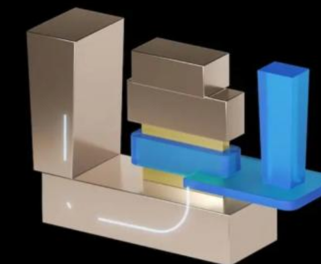
FD-SOI Transistor




FinFET Transistor

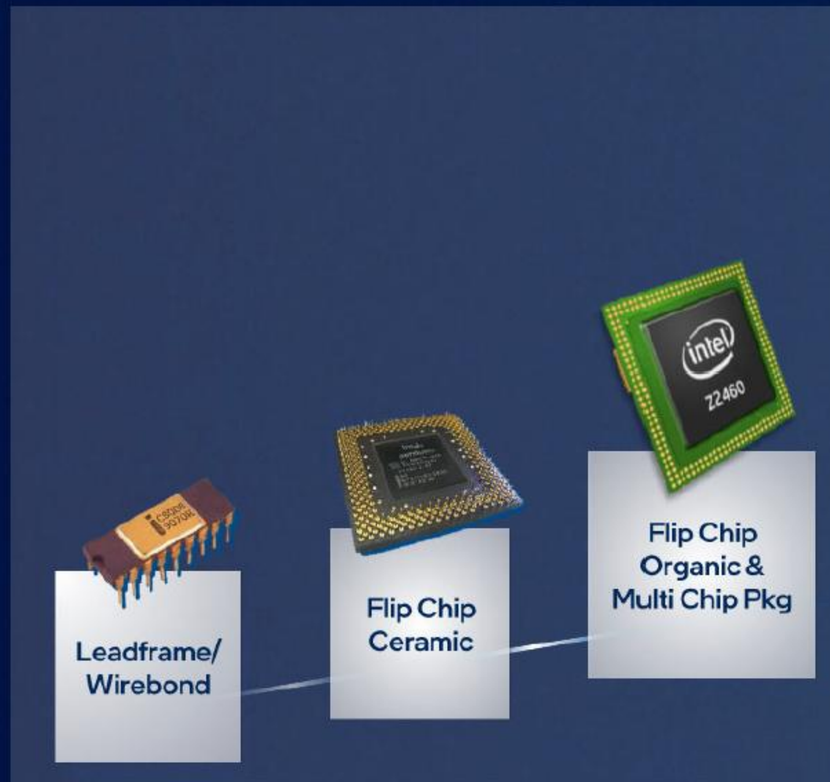


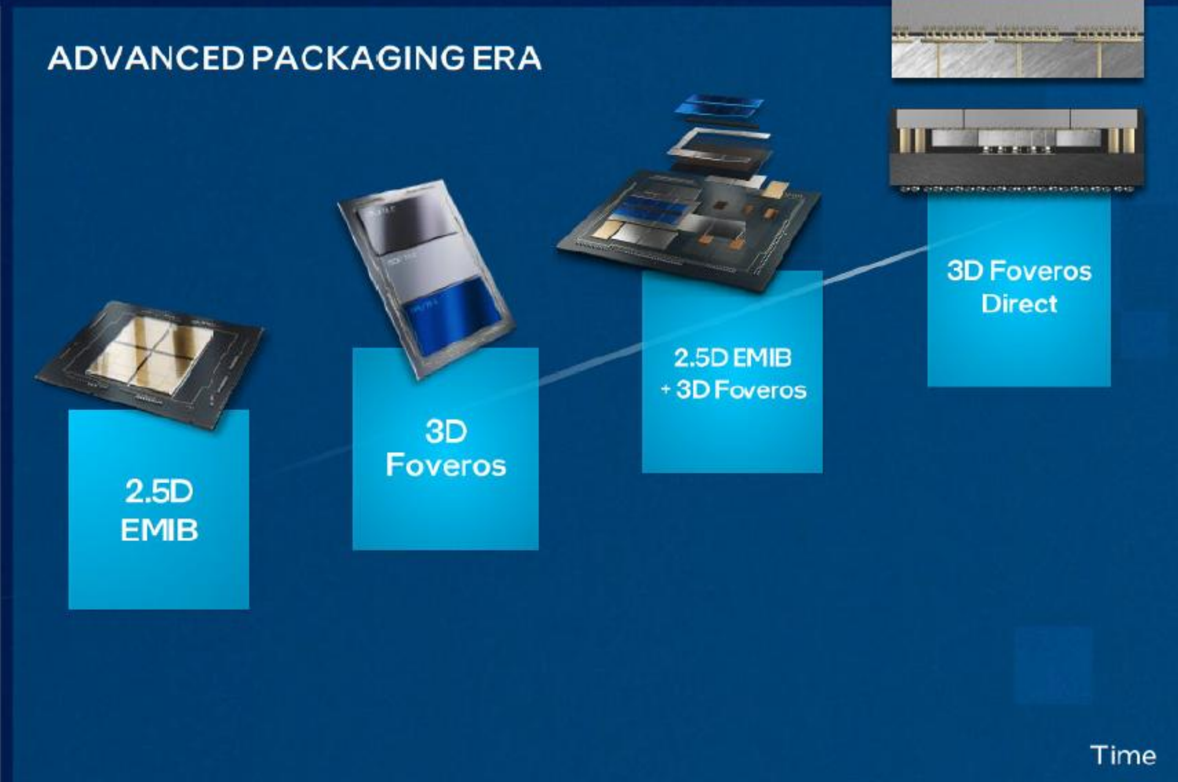
Samsung MBCFET



IBM & Samsung VFET

# EVOLUTION DES ASSEMBLAGES



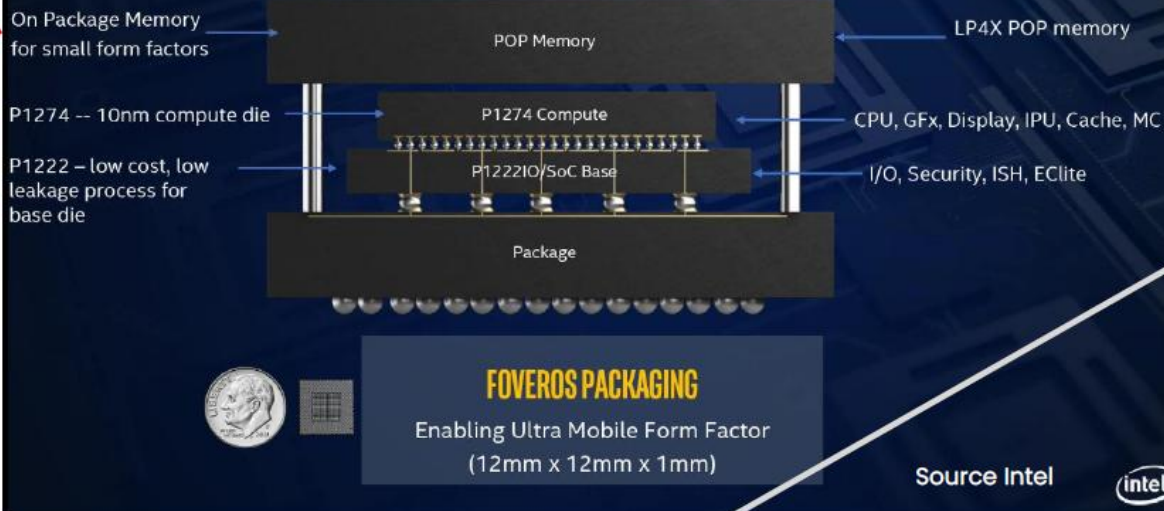



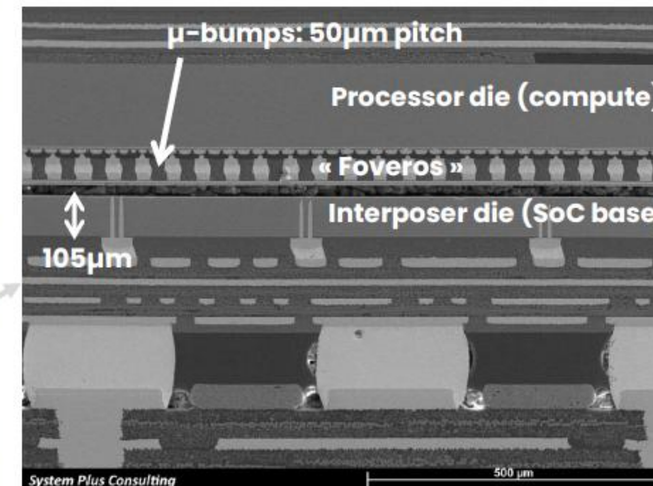

**Package main function:**
provide power and signaling from motherboard to die

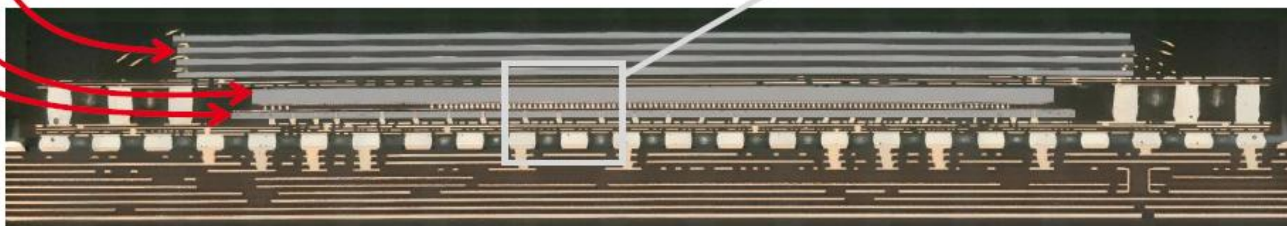
**Added package value:**
high density interconnects that enable larger die complexes from multiple process nodes

intel. Assembly Test Technology Development

# ASSEMBLAGE HÉTÉROGÈNE



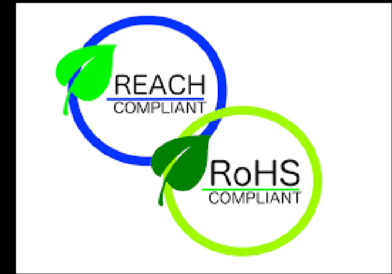



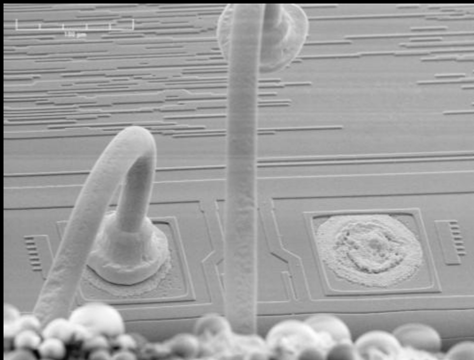



Source Yole SystemPlus

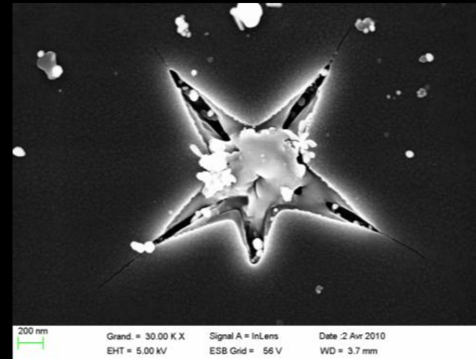
**DRAM stack**: CMOS 19nm DRAM
**PoP**: 3-layer PCB substrate
**Top die**: FinFET 10nm 13ML
**3D integration**: Foveros
**Bottom die**: FinFET 22nm 11ML
**Package**: 4-layer PCB substrate
**Board**: 10-layer PCB substrate

# DÉFAILLANCES

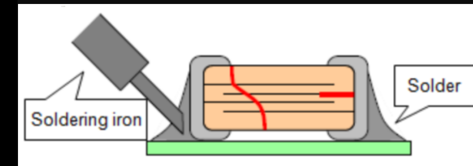


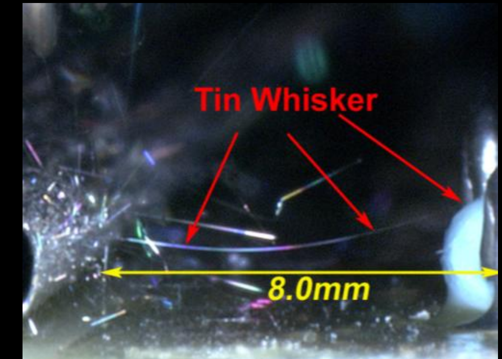
QUALITÉ




ROBUSTESSE




REPORT SUR CARTE

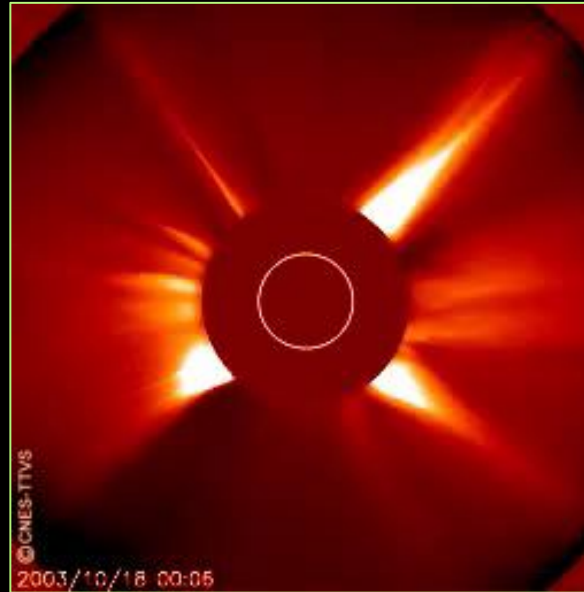



RÉGLEMENTATION

# ENVIRONNEMENT SPATIAL

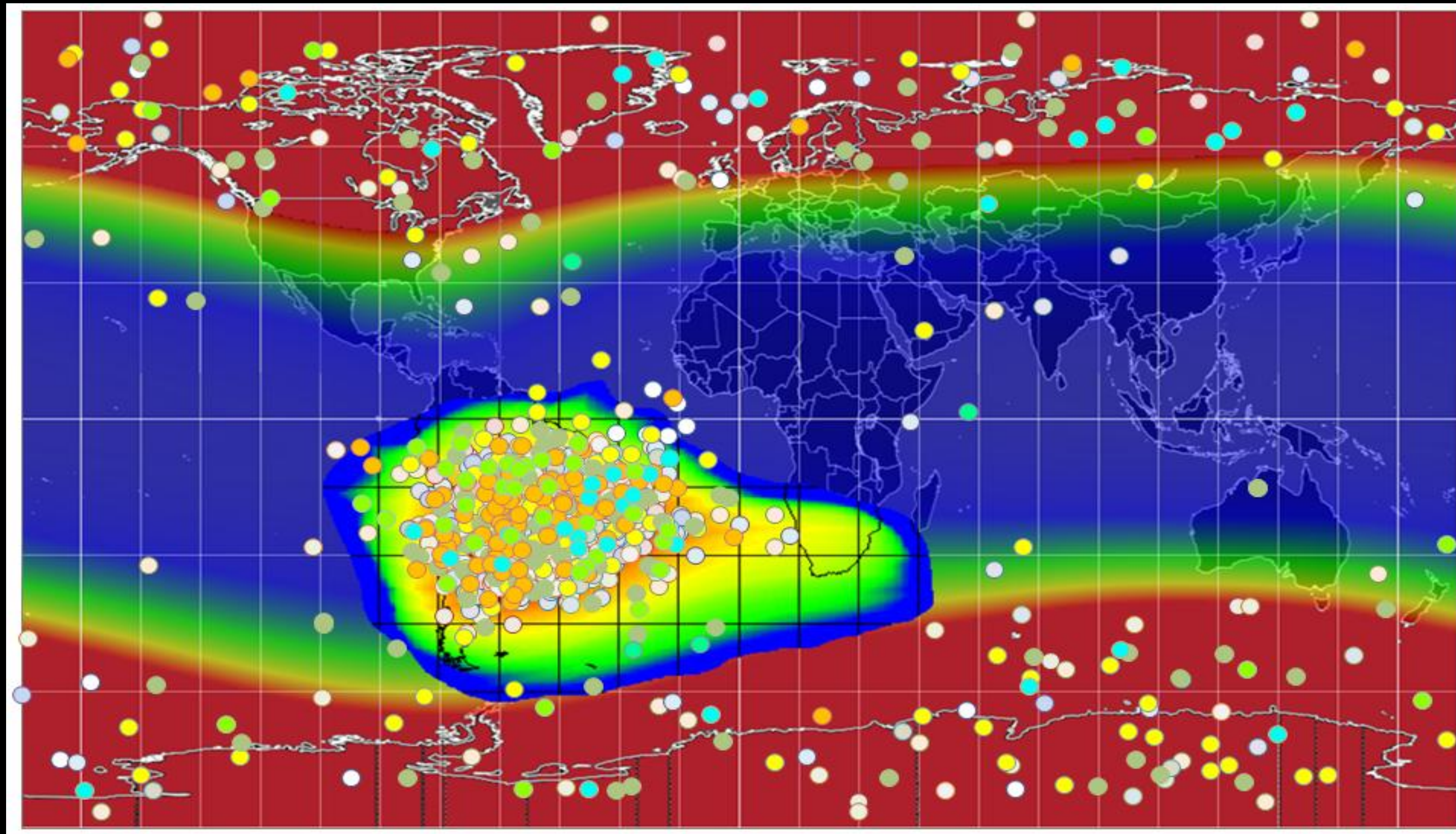
## Radiation belts

## Solar events




## Cosmic rays

# LOW EARTH ORBIT IN-FLIGHT FEEDBACK



**1028 unexpected behaviors, 10 LEO satellites**

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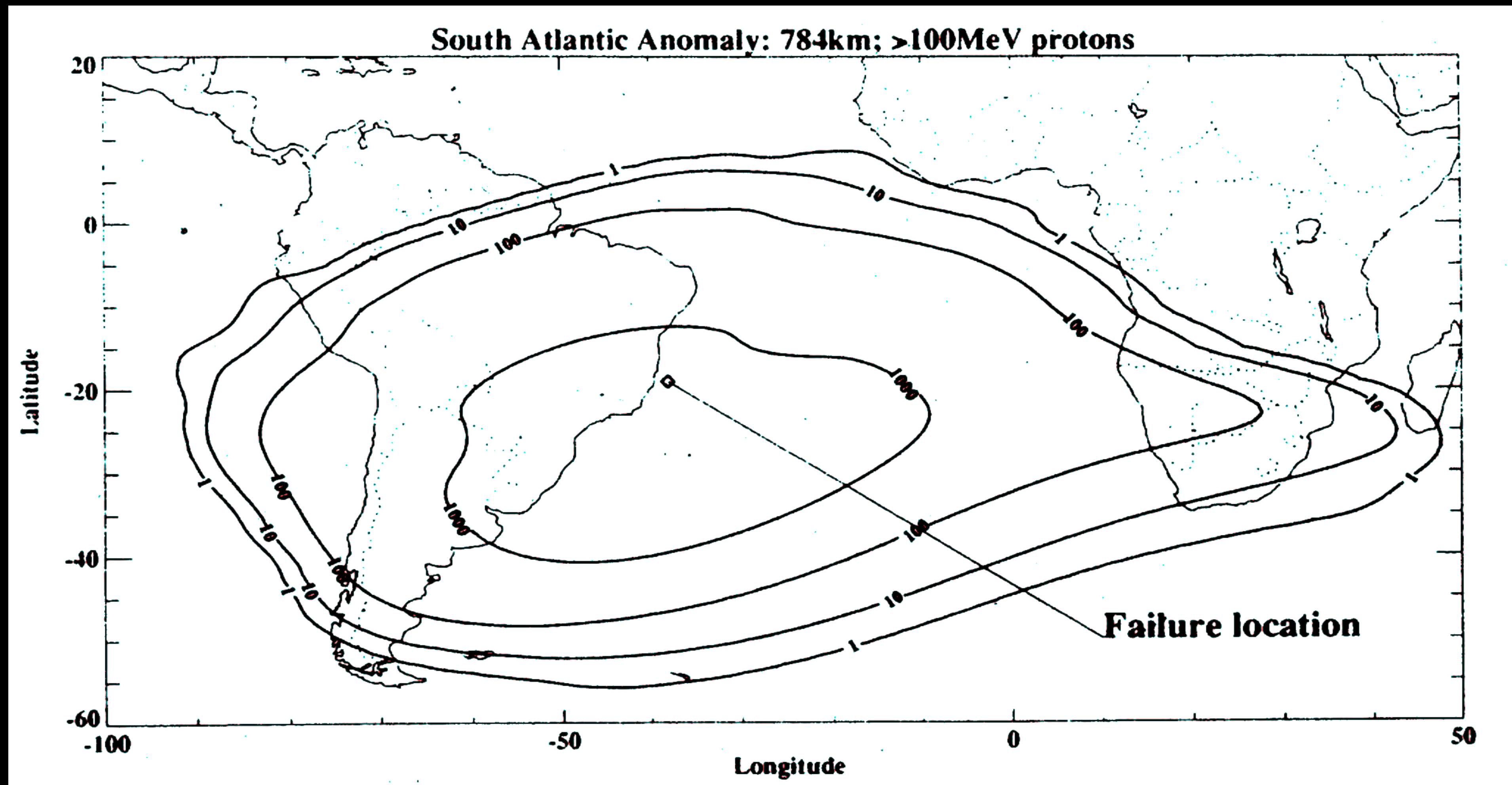
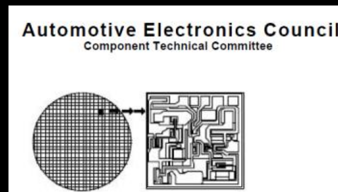
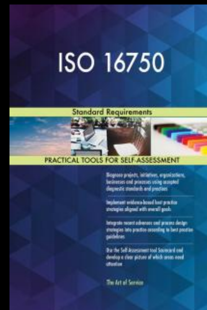
# CONSEQUENCES : ... TO DEADLY

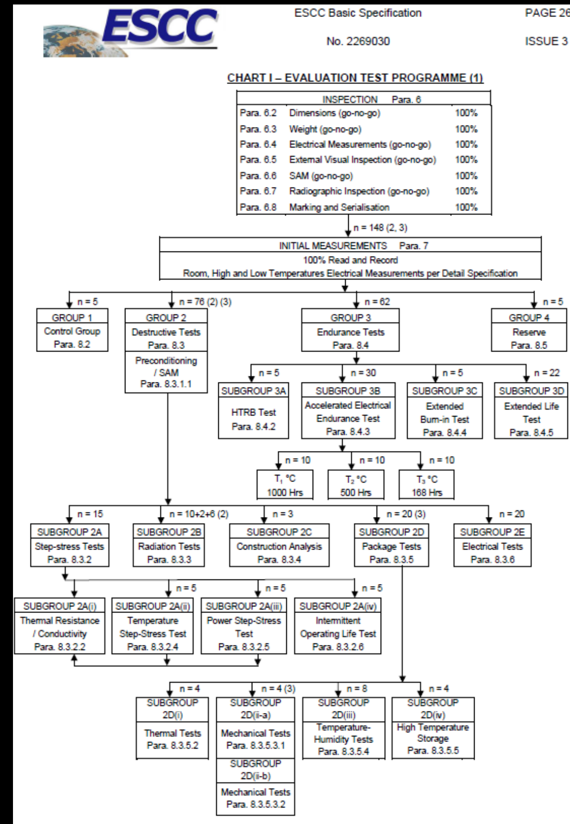


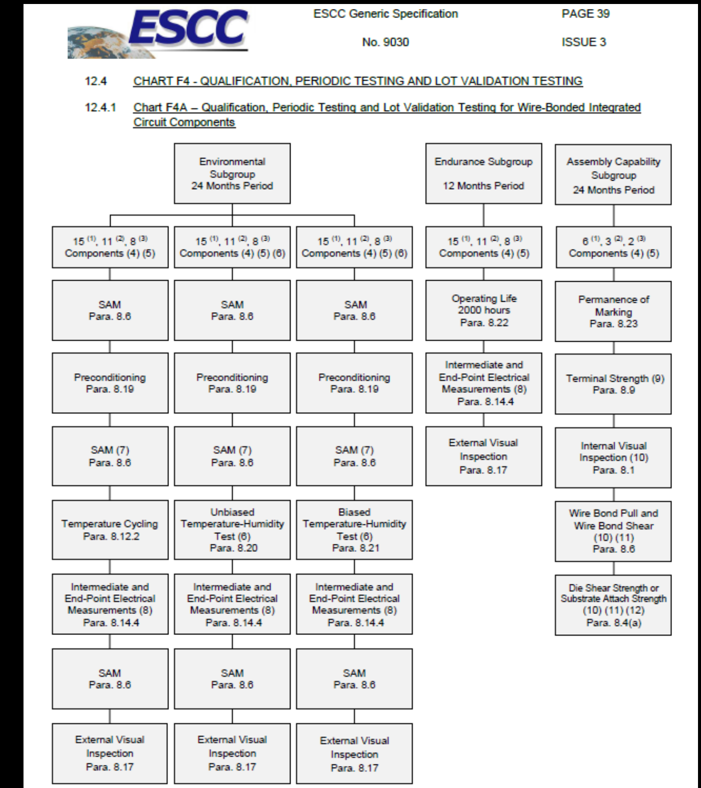

PRARE / ERS-1 instrument loss

# QUALIFICATION



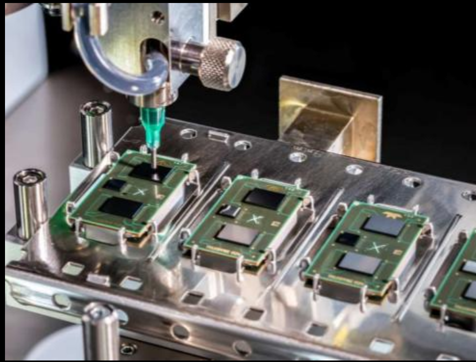




→Besoins de standards adaptés au nouvelles technologies :

GaN de Puissance , SiC, UDSM, Intégration 3D

# ENJEUX FIABILITÉ DE DEMAIN



CONNAISSANCE DES TECHNOLOGIES

Mécanisme de défaillances

Facteurs d'accélération

STANDARDS DE QUALIFICATION

ESSAIS ACCÉLÉRÉS

FIABILITÉ PRÉDICTIVE

Centre Français Fiabilité

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**Merci aux contributeurs CNES :**
**Robert Ecoffet, Jean-Baptiste Sauveplane, Guillaume Bascoul, Sophie Dareys**

# merci pour votre écoute !

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